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Performance Evaluation on the Basis of Energy in NoCs

Lalit Kishore Arora [#1], Rajkumar [*2]

[#] *MCA Dept, AKG Engg College,Ghaziabad, UP, India.*

[*] *CSE Dept, Gurukul Kangri Vishva Vidyalaya, Haridwar, UK, India.*

***Abstract*— The classical interconnection network topologies such as point-to-point and bus-based, recently has been replaced by the new approach Network-on-Chip (NoC). NoC can consume significant portions of a chip's energy budget, so analyzing their energy consumption early in the design cycle becomes important for architectural design decisions. Although numerous studies have examined NoC implementation and performance, few have examined energy. This paper determines the energy efficiency of some of the basic network topologies of NoC. We compared them, and results show that the CMesh topology consumes less energy than Mesh topology.**

Keywords*:* Network-on-Chip, Interconnection Networks, Topologies, Multi-core processor.

I. INTRODUCTION

In the design cycle of system-on-chip (SoCs) [20], the main emphasis is on the computational aspect. However, as the number of components on a single chip and their performance continue to increase, the design of the communication architecture plays a major role in defining the area, performance, and energy consumption of overall system. Furthermore, with technology scaling, the global interconnects cause severe on-chip synchronization errors, unpredictable delays, and high power consumption[27]. To remove these effects, the network-on-chip (NoC) approach emerged recently as a promising alternative to classical bus-based and point-to-point (P2P) communication architectures [31],[1],[25].

The remainder of this paper is organized as follows. Section 2 explains the related work and motivation behind this work. Section 3 describes the overview of the topologies which we have used in this experiment. In section 4 we describe the results of

experiments for both topologies for energy consumption.

II. MOTIVATION

To connect the increasing number of cores in a scalable way, researchers are evaluating packet-switched networks-on-chip (NoCs) [9], [10], [23]. The increasing disparity between wire and transistor delay [11] and the dependence between interconnect and memory system performance suggest that the relative importance of NoCs will increase in future CMP designs. As a result, there has been significant research in topologies [7], [16], [28], router microarchitecture [15], [21], wiring schemes [4], and power optimizations [32]. Nevertheless, there is a great need for further understanding of interconnects for large-scale systems at the architectural level. Previous studies also focused on CMPs [18], have used synthetic traffic patterns [7], [15], [21], or traces [28], or do not model the other components of the memory hierarchy [16].

In the previous paper [33] we determined the network energy efficiency for the Fat Tree and Mesh, and results shown that Mesh consumes less energy than the Fat Tree topology.

Here we determine the network energy efficiency (in pJ/bit) as a function of network bandwidth for networks with a fixed size of 64 nodes running different-different traffic patterns. We also changed the network bandwidth by changing the channel width. The four data point for each topology corresponds to channel width of 16, 24, 48, 72 bits.

III. TOPOLOGIES FOR EVALUATION

The topology defines how routers are connected with each other and the network endpoints. For a large-scale system, the topology has a major impact on the performance and cost of the network. our study aims to determine the energy consumed by network topologies across a range of network parameters including network bandwidth, traffic pattern, network frequency. In the experiments we study four realistic topologies the Mesh, the concentrated Mesh (CMesh).

A. Mesh Topology

Linear arrays are called 1-D meshes and they are incrementally scalable. When dealing with a mesh, we usually assume that its dimension *n* is *fixed*. If we want to change its size, we change the side lengths. The most practical meshes are, of course, *2-D* and *3-D* ones [6].

In a mesh network, the nodes are arranged in a k dimensional lattice of width w, giving a total of w^k nodes.[usually k=1 (linear array) or k=2 (2D array)

e.g. ICL DAP]. Communication is allowed only between neighboring nodes. All interior nodes are connected to 2k other nodes.

The most important mesh-based parallel computers are Intel's Paragon (2-D mesh) [14] and MIT J-Machine (3-D mesh). Also transputers used 2-D mesh interconnection. Processors in mesh-based machines are allocated by submeshes and the *submesh allocation* strategy must handle possible *dynamic fragmentation* and *compaction* of the global mesh network, similarly to hypercube machines [30].

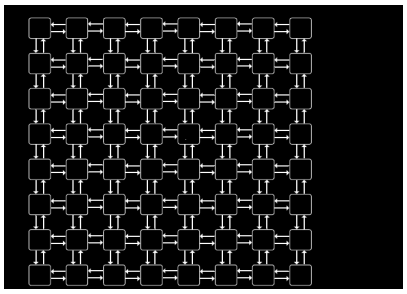

Figure-1. Mesh

B. CMesh Topology

The 2D mesh is a popular interconnect choice in large-scale CMPs [5], [14]. Each of the T/C routers connects to its four neighbouring routers and C source or destination nodes. T represents the number of sources and destinations in the network and degree of concentration C.

The degree of concentration C, in nodes per router, is typically applied to reduce the number of routers and therefore hops. In this way, mesh with a concentration factor, commonly referred to as CMesh.

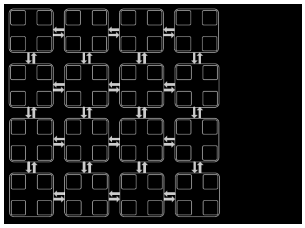

Figure-2. CMesh

The major advantage of the mesh is its simplicity. All links are short and balanced and the overall layout is very regular. The routers are low radix with up to C + 4 input and output ports, which reduces their area footprint, power overhead, and critical path. The major disadvantage is the large number of hops that flits have to potentially go through to reach their final destination (proportional to "N for N routers). Each router imposes a minimum latency (e.g., 3 cycles) and is a potential point of contention. A large number of hops has a direct impact on the energy consumed in the interconnect for buffering, transmission, and control. Hence, meshes could face performance and power scalability issues for large-scale systems. To address this shortcoming, researchers have proposed meshes with physical [8] or virtual [17] express links.

IV. EVALUATION

Our network-on-chip (NoC) topology study aims to determine the energy efficiency of network topologies across a range of network parameters including network bandwidth, traffic pattern, network frequency. In the experiments we compared the Mesh and CMesh topologies. In this experiment we used a RTL based router model and spice based channel model to obtain the energy results. The router RTL were place and routed using a commercial 45 nm lower power library running at 200MHz. The channel model uses technology parameters from the same library.

Figure-3 shows network energy efficiency (in pJ/bit) as a function of network bandwidth for networks with a fixed size of 64 nodes running uniform random traffic. We change the network bandwidth by changing the channel width. The four data point for each topology corresponds to channel width of 16, 24, 48, 72 bits. For each channel width configuration, the network is running at 50% of saturationbandwidth.

Figure 3 and 4 shows the effect of varying traffic patterns on the energy efficiency of both network topologies. Each network configuration is running at 50% saturation throughput under the test traffic pattern. Both Mesh and CMesh network topology uses dimension order routing. In figure 5, using dimension order routing under transpose traffic, much of the network infrastructure is idle except for few heavily loaded channels. As a result the energy per bit of Mesh topology increases.

In figure 5, nearest neighbour traffic heavily favours the mesh topology. Each node in the mesh has a dedicated channel to each of its immediate neighbours, this result in very high network bandwidth. For other one topology, nearest neighbour traffic under utilizes network resources such as the long channels of the Mesh. As a result, this under utilized resources decreases the energy efficiency of CMesh topology when compared to the Mesh.

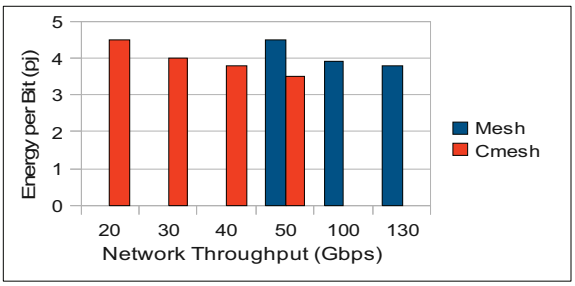

Fig. 3. Network energy per bit sent under uniform random traffic vs. network bandwidth

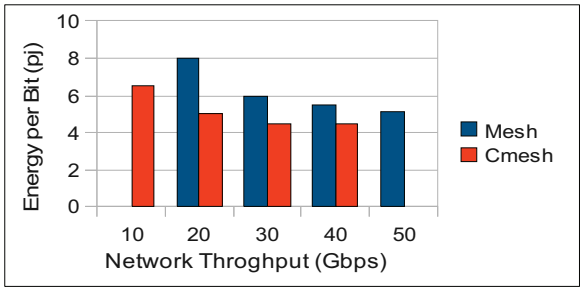

Fig. 4. Network energy per bit sent under transpose traffic vs. network bandwidth

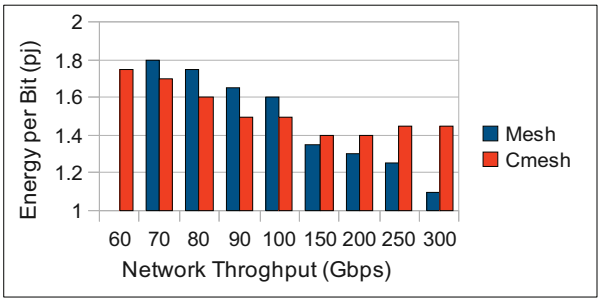

Fig. 5. Network energy per bit sent under nearest neighbour traffic vs. network bandwidth

V. CONCLUSION AND FUTURE SCOPE

As we discussed in [33] we have shown that Mesh gives better energy efficiency than the Fat Tree. Here we compared two another popular interconnection networks, Mesh and CMesh network topology. After evaluation Mesh and CMesh, in different traffic patterns we found that CMesh topology consumes less energy than Mesh topology as shown in different charts. In future we are trying to evaluate two more topologies CMesh and FBFly with above traffic patterns.

REFERENCES

[1] *Hemani, et al., "Network on Chip: An Architecture for Billion Transistor Era," In Proc. IEEE NorChip Conf., Nov. 2000.*

[2] *ARG Database CD, http://amalfi.dis.unina.it/.T. Messmer, H. Bunke, "A Decision Tree Approach to Graph and bgraph Isomorphism Detection," Pattern Recognition, Dec. 1999.*

[3] *BALASUBRAMONIAN, R., MURALIMANOHAR, N., RAMANI, K., AND VENKATACHALAPATHY, V. Microarchitectural wire management for performance and power in partitioned architectures. In Proceedings of the 11th International Symposium on High-Performance Computer Architecture. IEEE, Los Alamitos, CA, 2005.*

[4] *BELL, S., EDWARDS, B., AMANN, J., CONLIN, R., JOYCE, K., LEUNG, V., MACKAY, J., REIF, M., BAO, L., ET AL. TILE64 processor: A 64-core SoC with mesh interconnect. In Proceedings of the International Solid-State Circuits Conference. IEEE, Los Alamitos, CA,2008*

[5] *Benini, L.; De Micheli, G., "Networks on chips: a new SoC paradigm", IEEE Computer Society , Computer, 70 – 78, Jan 2002.*

[6] *BONONI, L., CONCER, N., GRAMMATIKAKIS, M., COPPOLA, M., AND LOCATELLI, R. NoC topologies exploration based on mapping and simulation models. In Proceedings of the 10th Conference on Digital System Design Architectures, Methods and Tools. IEEE, Los Alamitos, CA. 2007.*

[7] *DALLY, W. Express cubes: Improving the performance of k-ary n-cube interconnection networks. IEEE Trans. Comput. 40, 9, 1016–1023. 1991.*

[8] *DALLY, W. J. AND TOWLES, B. Route packets, not wires: On-chip interconnection networks. In Proceedings of the 38th Conference on Design Automation. ACM, New York, 2001.*

[9] *DE MICHELI, G. AND BENINI, L. Networks on chip: A new paradigm for systems on chip design. In Proceedings of the Conference on Design, Automation and Test in Europe. ACM, New York, 2002.*

[10] *HO, R., MAI, K., AND HOROWITZ, M. The future of wires. Proc. IEEE. 89, 4, 24. ,2001*

[11] *http://csrc.nist.gov/CryptoToolkit/aes/rijndael/*

[12] *http://vlado.fmf.uni-lj.si/pub/networks/pajek/*

[13] *Intel Tera-scale Computing Research Program. http://www.intel.com/go/terascale ,2008.*

[14] *KIM, J., PARK, D., THEOCHARIDES, T., VIJAYKRISHNAN, N., AND DAS, C. R. A low latency router supporting adaptivity for on-chip interconnects. In Proceedings of the 42nd Annual Conference on Design Automation. ACM, New York, 2005.*

[15] *KIM, M. M., DAVIS, J. D., OSKIN, M., AND AUSTIN, T. Polymorphic on-chip networks. In Proceedings of the 35th Annual International Symposium on Computer Architecture. ACM, New York.2008.*

[16] *KUMAR, A., PEH, L.-S., AND JHA, N. K. Token flow control. In Proceedings of the 41th Annual International Symposium on Microarchitecture. IEEE, Los Alamitos, CA, 2008..*

[17] *KUMAR, R., ZYUBAN, V., AND TULLSEN, D. M. Interconnections in multi-core architectures: Understanding mechanisms, overheads and scaling. In Proceedings of the 32nd Annual International Symposium on Computer Architecture. ACM, New York, 2005..*

[18] *LEISERSON, C E, "Fat-trees - University networks for hardware-efficient supercomputing" , IEEE Transactions on Computers. Vol. C-34, pp. 892-901. Oct. 1985.*

[19] M. Kreutz, et. al. "Communication Architectures for System-On-Chip," In 14th Symp. on Integrated Circuits and Systems Design, Sep. 2001.
[20] MULLINS, R., WEST, A., AND MOORE, S. Low-latency virtual-channel routers for on-chip networks. In Proceedings of the 31st Annual International Symposium on Computer Architecture. ACM, New York, 2004..
[21] Ohring, S.R.; Ibel, M.; Das, S.K.; Kumar, M.J., "On generalized fat trees", in proceedings Parallel Processing Symposium, 1995.
[22] OWENS, J. D., DALLY, W. J., HO, R., JAYASIMHA, D. N., KECKLER, S. W., AND PEH, L.-S. Research challenges for on-chip interconnection networks. IEEE Micro. 27, 5, 96–108. 2007.
[23] P. Foggia, et al., "A Performance Comparison of Five Algorithms for Graph Isomorphism," In Proc. 3rd IAPR TC-15 Workshop on Graphbased Representations in Pattern Recognition, May, 2001.
[24] P. Guerrier, A. Greiner, "A Generic Architecture for On-Chip Packet Switched Interconnections," In Proc. DATE, March 2000.
[25] Pierre Guerrier, Alain Greiner, "A generic architecture for on-chip packet-switched interconnections", Proceedings of the conference on Design, automation and test in Europe,pp 250 – 256, 2000
[26] S. Murali, G. De Micheli, "SUNMAP: A Tool for Automatic Topology Selection and Generation for NoCs," In Proc. 41st DAC, June 2004.
[27] TOTA, S., CASU, M. R., AND MACCHIARULO, L. 2006. Implementation analysis of NoC: a MPSoC trace-driven approach. In Proceedings of the 16th Great Lakes Symposium on VLSI. ACM, New York.V.S. Adve, M.K.
[28] Vernon , "Performance analysis of mesh interconnection networks with deterministic routing", IEEE
[29] Transactions on parallel and distributed systems, vol. 5, no3, pp. 225-246, 1994.
[30] VS Adve, MK Vernon, "Performance analysis of multiprocessor mesh interconnection networks with wormhole routing", Computer Sciences Technical Report #1001a, June ,1992.
[31] W. Dally and B. Towles, "Route packets, not wires: On-chip interconnection networks," In Proc. 38th DAC, June 2001.
[32] WANG, H., PEH, L.-S., ANDMALIK, S. Power-driven design of router microarchitectures in onchip networks. In Proceedings of the 36th Annual International Symposium on Microarchitecture. IEEE, Los Alamitos, CA 2003..
[33] LALIT K. ARORA, RAJKUMAR, Network-on-Chip Evaluation Study for Energy, Proceeding of International conference on Reliability, Infocom Technology and Optimization, Lingaya's University, India, pg 314-320, Nov,2010